Educator Insights: A Journal of Teaching Theory and Practice
Volume 2, Issue 3, March 2026
brightmindpublishing.com
ISSN (E): 3061-6964

PHYSICAL FOUNDATIONS OF THE FERROELECTRIC EFFECT AND ANALYSIS OF ITS APPLICATIONS IN THE MODERN MICROELECTRONICS INDUSTRY

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Abstract

The article analyzes the microscopic mechanisms determining the physical nature of ferroelectric materials and thermodynamic models of phase transitions. The significance of thin-film structures based on hafnium oxide (HfO_2) in modern industry, specifically in microelectronics, is highlighted. The study provides a scientific basis for the prospects of utilizing the negative capacitance effect and ferroelectric tunnel junctions in neuromorphic computing systems.

Keywords: Ferroelectricity, polarization, perovskite, hafnium oxide, negative capacitance, memristor, Curie temperature, dielectric permittivity.

Introduction

In modern condensed matter physics, ferroelectric materials occupy a unique position due to their extraordinary electrophysical properties. Ferroelectricity is a phenomenon of spontaneous polarization arising from the symmetry breaking of the crystal lattice. Over the last decade, as the dimensions of microprocessors and memory devices have scaled down to the nanometer range, the physical limits of conventional dielectrics have become increasingly apparent.

This article utilizes the Landau-Ginzburg-Devonshire (LGD) phenomenological theory and crystallographic analysis methods to characterize the ferroelectric state. The comparison of the electrophysical parameters of materials is based on experimental data from recent years (2021–2026) and meta-analyses from the Scopus database.

In ferroelectric materials, the phase transition is expressed through the expansion of the free energy density (G) in terms of the polarization (P):

$$G = G_0 + \frac{1}{2}\alpha P^2 + \frac{1}{4}\beta P^4 + \frac{1}{6}\gamma P^6 - E \cdot P$$

where $\alpha = \alpha_0(T - T_C)$. When the temperature drops below the Curie point ($T < T_C$) becomes negative ($\alpha < 0$), and the system transitions into a stable spontaneous polarization state [1]. The dynamics of domain walls and their displacement under the influence of an external field determine the dielectric permittivity of the material [6].

This process is particularly evident in the following directions:

The integration of Hafnium Oxide (HfO_2)) and Complementary Metal-Oxide-Semiconductor (CMOS) technology: The primary driver of this renaissance has been the discovery of ferroelectricity in hafnium oxide, which is compatible with conventional semiconductor technology [1]. Due to its high compatibility with silicon, this material is becoming an integral part of CMOS logic elements and memory devices. Uzbek scientists are also researching the significance of HfO_2-based structures as a foundation for nanoelectronics [6].

Memory based on ferroelectric materials is distinguished not only by its high speed but also by its exceptional energy efficiency. Currently, the future of this technology is envisioned through its integration into 3D NAND structures [3]. Furthermore, the application of ferroelectric dielectrics in sensor technology has further enhanced their practical significance [10].

3D NAND is a technology that involves arranging transistors vertically, in a "multi-story building" configuration, to increase the capacity of data storage memory chips. In traditional 2D NAND technology, memory cells were arranged only on a single plane (side-by-side). Beyond a certain point, bringing the cells too close to each other led to electrical interference and data loss. 3D NAND was specifically developed to overcome this "density wall."

In the 3D NAND architecture, transistor layers are stacked vertically. Currently, the industry is producing chips with 176, 232, or even more layers. In this process, vertical holes (channels) are etched through the layers and filled with semiconductor material. Data reading and writing operations are performed through these channels. Each floor contains horizontal conductive layers that activate specific memory cells.

As highlighted in the research by T. Mikolajick and S. Slesazeck (2025) [3], the future of 3D NAND technology is closely linked to ferroelectric materials, particularly hafnium oxide (HfO_2). While current 3D NAND utilizes a "charge trap" mechanism, the integration of a ferroelectric layer makes the memory significantly faster and requires lower voltage for data retention. The nanometer-scale thickness of the ferroelectric layer allows for even denser vertical stacking of 3D NAND layers.

The primary advantages of this technology include:

High Density: It stores dozens of times more data in the same area compared to 2D NAND (resulting in SSDs with multi-terabyte capacities).

Reduced Interference: Since the distance between cells is greater in the vertical direction, electron leakage and mutual interference are minimized.

Parallelism: Data can be read simultaneously from multiple layers.

In microelectronics, while traditional materials like $\mathrm{Pb(Zr,Ti)O_3}$ (PZT) or $SrBi_2Ta_2O_9$ (SBT) lose their ferroelectric properties at dimensions below 10 nm, hafnium oxide ($\mathrm{HfO_2}$) has become an integral part of CMOS (Complementary Metal-Oxide-Semiconductor) technology since 2011 [1]. CMOS is the foundational technology for manufacturing the integrated circuits that power modern electronics.

Specifically, $\mathrm{HfO_2}$ thin films maintain their orthorhombic ($\mathrm{Pca2_1}$) phase even at thicknesses of 3–5 nm, enabling the creation of memory elements at the nano-scale [6].

Due to the negative capacitance effect, it has become possible to reduce the gate voltage of the transistor to 0,5 V and lower the Subthreshold Swing **(SS)** below the 60mV/dec limit [2]. The Subthreshold Swing is a critical parameter that indicates how quickly and efficiently a field-effect transistor (FET) transitions from the “OFF” state to the “ON” state. In simple terms, it represents how much the control voltage must be changed to fully “activate” the transistor.

Even when the voltage is below the threshold voltage **(**V_{th}**)**, a very small amount of current still flows through the transistor. This region is known as the subthreshold region. The Subthreshold Swing is defined as the amount of millivolts (mV) required to increase the current by 10 times (one decade). Its unit is mV/dec.

For a transistor approaching ideal characteristics, the Subthreshold Swing is determined by the following formula:

$$\mathrm{SS} = \ln{(10)} \cdot \frac{kT}{q} \cdot \left(1 + \frac{C_d}{C_{ox}}\right)$$

where:kT/q — is the thermal voltage (26 mV at room temperature), C_d — is the depletion layer capacitance, C_{ox} — is the oxide layer capacitance.

At room temperature (T = 300 K), the minimal theoretical value of the Subthreshold Swing **(SS)** for classical MOSFETs is 60mV/dec. This implies that a minimum voltage change of 60 mV is required to increase the current by a factor of ten. Falling below this threshold is physically impossible for conventional transistors; hence, it is referred to as the "thermionic limit" (or Boltzmann tyranny).

The smaller the SS value (e.g., 65 – 70 mV/dec), the "sharper" and more responsive the transistor operates, leading to significantly lower power consumption. Conversely, a high SS value causes the transistor to leak substantial current even in the "OFF" state. This is particularly detrimental to battery-powered communication devices, leading to rapid energy depletion. As transistor dimensions scale down to the nanometer level, maintaining a stable SS becomes increasingly challenging.

In modern 3D NAND or FinFET (tri-gate) transistors, the gate surrounds the channel from three or four sides. This enhanced electrostatic control over the channel helps bring the SS value closer to the ideal 60 mV/dec.

Analysis indicates that ferroelectrics are currently leading in the following strategic directions:

1. NCFET (Negative Capacitance Field-Effect Transistor): A semiconductor device that utilizes ferroelectric materials to enhance the energy efficiency of traditional transistors. NCFET is a field-effect transistor that exploits the "negative capacitance" effect. These transistors prevent processors from overheating and can reduce power consumption by 30%–40% [2].

NCFET was conceived to bypass the aforementioned "thermionic limit" and drastically reduce the power consumption of processors (for instance, extending smartphone battery life).

In the NCFET structure, an ultra-thin ferroelectric layer (typically hafnium oxide — HfO_2) is integrated into the transistor gate along with a conventional dielectric. Under specific conditions, the ferroelectric material transitions into a "negative capacitance" state. In this state, it internally amplifies the external gate voltage. Consequently, a much lower external voltage is sufficient to switch the transistor "ON", as the ferroelectric layer effectively "magnifies" this potential for the transistor channel.

The primary advantages of NCFET devices include:

Energy Efficiency: The **SS** value drops below 60 mV/dec (reaching 35 – 40 mV/dec), allowing processors to consume 30% – 40% less power.

Low-Voltage Operation: While modern chips operate at 0,8 – 1,2V, NCFET technology enables operation at 0,3 – 0,5 V.

High Performance: Despite the lower voltage, the operating frequency does not decrease; rather, efficiency-driven performance gains are possible.

Currently, industry giants such as Intel, Samsung, and TSMC are conducting research on implementing NCFET elements in 2nm and beyond process nodes. This technology is particularly promising for Artificial Intelligence (AI) chips and wearable devices (smartwatches, sensors).

2. FeRAM (Ferroelectric Random Access Memory): A type of memory that utilizes the ferroelectric effect to store data, offering non-volatile storage with write speeds measured in nanoseconds [3].

FeRAM is a high-speed, low-power, non-volatile memory. In simple terms, it functions as fast as DRAM (Dynamic Random Access Memory) but retains data without power, similar to NAND Flash.

DRAM: The volatile temporary storage (RAM) of computers and smartphones where data is processed rapidly by the processor.

NAND Flash: The non-volatile storage backbone of modern SSDs and flash drives, capable of retaining data for long periods without electricity.

FeRAM is considered a “universal memory” as it combines the best attributes of both high-speed volatile and non-volatile memories. The basic FeRAM memory block consists of a transistor and a ferroelectric capacitor.

Unlike a conventional capacitor, a FeRAM cell contains a ferroelectric layer within the capacitor structure. The physical basis of its operation is as follows:

Data Writing: Under the influence of an electric field, the central atom within the ferroelectric crystal (e.g., a Hafnium or Titanium ion) shifts “upward” or “downward”.

Data Retention: This atom maintains its position even when the external power is disconnected. Consequently, the memory is inherently non-volatile.

Logical States: The "upper" position of the ion represents a logical “1”, while the “lower” position represents a logical “0”.

FeRAM offers several significant advantages compared to the currently widespread Flash and DRAM memories (Table 1).

Table 1. Comparative Analysis of Memory Technologies

Feature	FeRAM	Flash (NAND)	DRAM
Non-volatility	Yes (Persistent)	Yes (Persistent)	No (Volatile)
Write Speed	Very High (ns)	Low (ms)	Very High (ns)
Endurance (Cycles)	10^{12} - 10^{14}	10^{3} - 10^{5}	Unlimited
Power Consumption	Very Low	High	Medium

The primary “drawbacks” of FeRAM are its lower storage density and currently higher manufacturing costs. Therefore, it cannot yet replace 256 GB storage modules in smartphones; however, it remains an irreplaceable technology in specialized fields.

Currently, FeRAM is widely utilized in the following sectors:

1.Automotive Industry: For instantaneous data logging in airbag systems and onboard computers.

2. Industrial Sensors: In devices that require continuous data recording under frequent power fluctuations.

3. Smart Cards: In bank cards and electronic passports due to its minimal power consumption.

4. Military and Aerospace Technology: FeRAM is highly valued as a radiation-hardened and exceptionally reliable memory type.

CONCLUSION

Based on the conducted analysis, it can be concluded that ferroelectric materials will define the future architecture of nanoelectronics. Specifically, the synthesis of lead-free materials ensures environmental safety [4]. Future research should focus on enhancing the resilience of these materials to radiation and extreme temperatures, particularly through structures based on aluminum scandium nitride (AlScN) [8]. Such structures are currently vital for the compact and reliable storage of large datasets in data centers and military communication systems.

The transition to lead-free materials for converting mechanical energy into electricity via the piezoelectric effect has become a global trend [4]. Through domain wall engineering, giant piezoelectric coefficients are being achieved in oxide-based ferroelectrics [7]. For high-temperature electronics, a new class of materials, such as AlScN, is being proposed [8].

In neuromorphic systems based on the operational principles of the human brain, ferroelectric materials are considered the most promising candidates for creating synaptic devices [5]. This technology, leveraging the negative capacitance effect, allows transistor power consumption to be reduced below conventional physical limits [2].

At the current stage of CMOS technology, the integration of ferroelectric layers (e.g., in FeFETs — Ferroelectric Field-Effect Transistors) is expanding device functionality. This historical progression is inextricably linked to the developmental history and technology of ferroelectric ceramics [10].

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